Ka-BAND MONOLITHIC GaAs FET POWER AMPLIFIER MODULES

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ABSTRACT

Monolithic GaAs FET power amplifiers consisting of several power combined devices have been fabricated and evaluated. The baseline monolithic chip design consists of a single stage 400 µm FET amplifier and a six-way travelling-wave power divider/combiner with a single stage amplifier in each of the six arms. Several chip combinations were used to make a 1 W amplifier with 5 dB gain and a 0.55 W amplifier with 27 dB gain at 34 GHz.

INTRODUCTION

Recent advances in GaAs power FET technology have made it possible to build power amplifiers at Ka-band (1,2). The results published so far use relatively small gate width devices (400 µm) and the maximum power obtained under compression is 0.2 W. For most applications more power and gain is required to satisfy the systems needs. This article describes a monolithic power combining scheme that uses several of these 400 µm devices in a six-way traveling-wave monolithic divider combiner to make a 0.6 W amplifier at 34 GHz with 2.8 dB gain. Modules with several cascaded stages producing 0.55 W with 27 dB gain at 34 GHz will be described. A two-way hybrid combining scheme making use of the 0.6 W monolithic chips producing 1 W of output power will also be described.

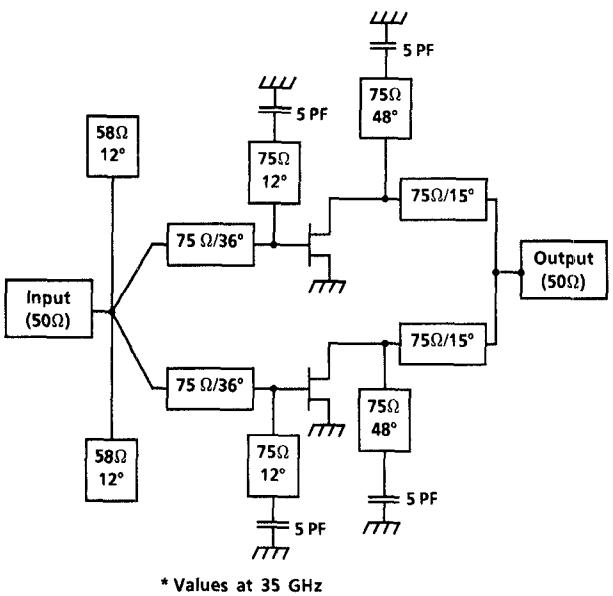

Figure 1. Schematic showing the circuit elements for the Ka-band monolithic unit cell consisting of two 200 µm FETs.

UNIT CELL MONOLITHIC DESIGN

The design of the power amplifiers described in this article revolves around a 400 µm monolithic unit cell. This cell is a modification on the cells described earlier in the literature (1,2). An equivalent circuit of the monolithically matched unit cell is shown in Figure 1. This unit cell uses two 200 µm FETs with overlay source grounding. Two smaller FETs are used rather than a single 400 µm FET to decrease the source lead inductance and therefore increase the gain. The major design difference from the power amplifier cells reported earlier is that the input uses open circuited stubs rather than MIM capacitors for matching purposes. This change was implemented to facilitate the position of the capacitors and to improve the yield. Matching is achieved on the input side by using an inductor to ground at the device and an open circuited stub 300 µm away from the device. The output is matched by using an inductor to ground at the device. The respective line lengths and impedances are given in the equivalent circuit of Figure 1.

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A picture of the monolithic unit cell is shown in Figure 2. The maximum power performance achieved under compression for this unit cell is 200 mW with 3.8 dB gain and 21% efficiency. At the 1 dB compression point the best cells produce 170 mW (22 dBm) with 5 dB gain. Realistically taking into consideration some mismatch losses and the average device performance the unit cell produces 126 mW (21 dBm) with 5 dB gain at the 1 dB compression point. The gain curve for the average unit cells at different power levels and bias conditions is given in Figure 3.

SIX-WAY COMBINED MONOLITHIC CHIP DESIGN

The design of this Ka-band power amplifier chip makes use of power combining schemes since large devices tend to be difficult to match. The monolithic chip consists of six 400 µm unit cells that are power combined using a six-way travelling-wave divider/combiner as shown in Figure 4. The monolithically combined chip takes advantage of device uniformity due to the close proximity of the single stage amplifiers. The travelling-wave divider/combiner (3,4) is ideal for monolithic design since it is compact and has broad-band and low-loss characteristics.

The design was implemented on 100 µm thick semi-insulating GaAs substrate and the total chip size is 19 mm^2, half of which is occupied by the divider/combiner. The total loss for the divider/combiner has been measured to be 2 dB at 34 GHz. This implies 1 dB loss in the divider and 1dB in the combiner. The performance of the six-way combined chip is shown in Figure 5. Under power conditions the chip can deliver 0.6 W (27.8 dBm) with 2.8 dB gain and 8.5% power-added efficiency. When comparing this data to the single unit cell performance one finds that only about .2 dB of gain is lost due to phase mismatch of the amplifier cells. This justifies the importance of monolithic combining since the adjacent devices are virtually identical. From a design stand point a higher gain cell would have been more appropriate to off set the divider loss. Under lower power conditions and with the bias adjusted for maximum gain the chip has 5 dB gain with 0.32 W (25 dBm) power output.

FIVE STAGE AMPLIFIER DESIGN

In order to achieve a high gain power module a five stage amplifier using single stage monolithic devices was designed. Due to power consumption considerations one can only use the six-way combined chip in the final two stages of the amplifying chain. For more efficient operation the earlier stages should be made using smaller devices. In this design the first three stages were made using the same 400 µm unit cells used in the combined chip. These chips are monolithically matched to 50 ohms and have an input and output return loss better than 13 dB which makes them easy to cascade. The last two stages of the module were made using the six-way combined chip described earlier. In the case of this chip the input and output return loss is less than 18 dB since the

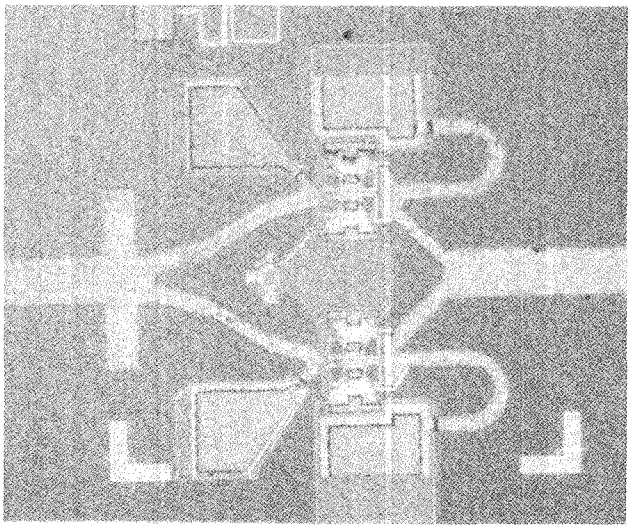

Figure 2. Picture of the Ka-band monolithic unit cell consisting of two 200 µm FETs.

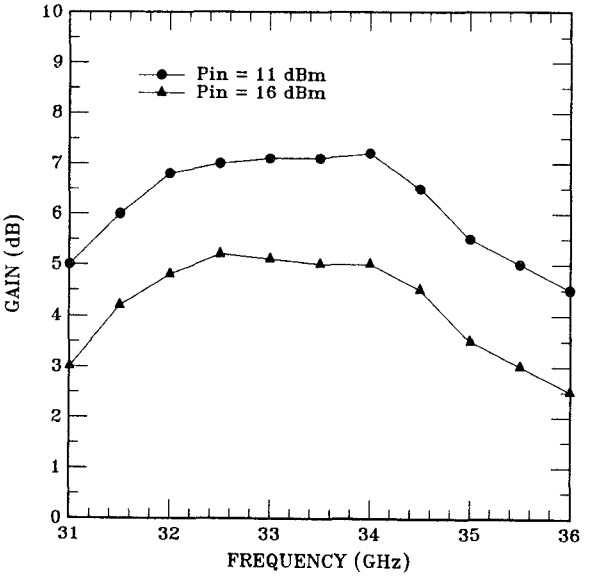

Figure 3. Typical gain curve for the average Ka-band monolithic unit cell.

divider/combiner has resistors to absorb any mismatches. This makes the chips easy to cascade.

This hybrid module using monolithic chips is shown in Figure 6. Due to biasing considerations dc blocking capacitors were used to isolate the respective stages. Since the amplifier stages in this design are not

at the same power level, separate bias for each stage was used to optimize the gain. The performance of this five stage amplifier is shown in Figure 7. Under power conditions the chip can deliver 0.55 W (27.5 dBm) with 27.5 dB gain and 6.1% power-added efficiency. Under lower power conditions and with the bias adjusted for maximum gain the chip has 31 dB gain with 0.4 W (26 dBm) power output.

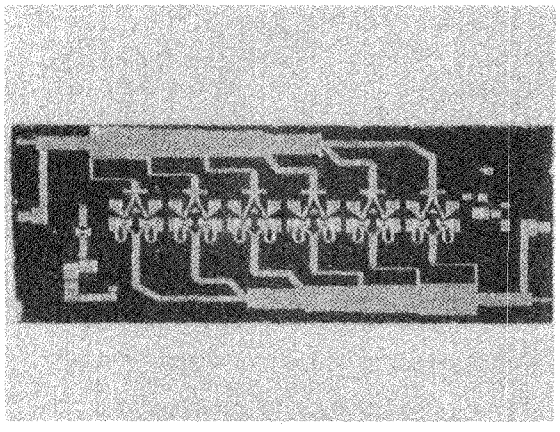

Figure 4. Picture for the monolithic GaAs six-way combined Ka-band amplifier chip.

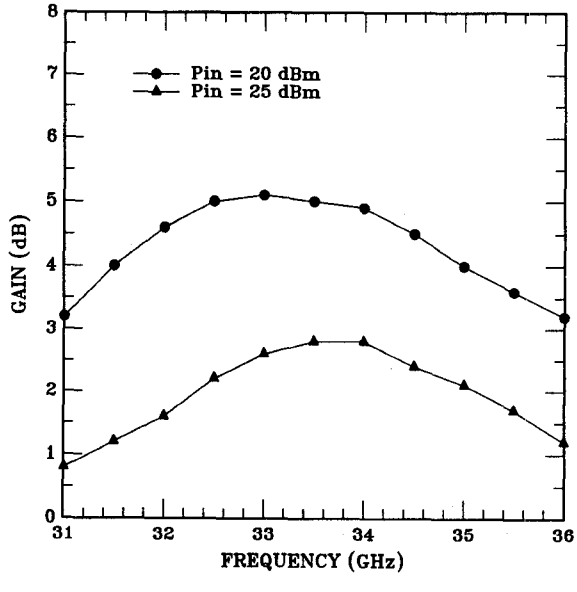

Figure 5. Gain curve for the monolithic GaAs six-way combined chip.

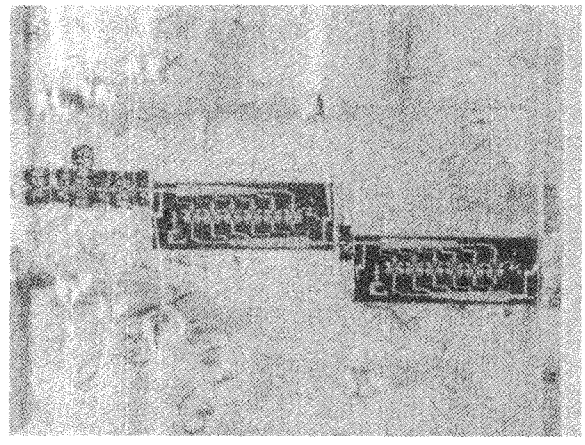

Figure 6. Picture for the five stage Ka-band high gain power amplifier module.

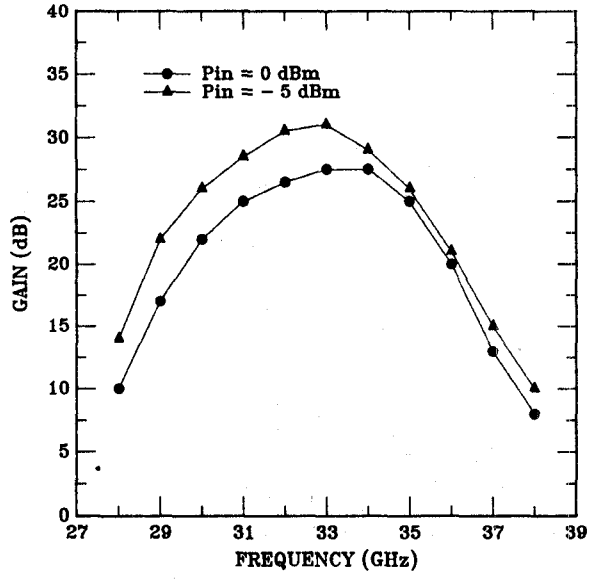

Figure 7. Gain curve for the five stage power amplifier module.

1 WATT POWER AMPLIFIER DESIGN

The 1 W amplifier design was implemented using two levels of power combining. The first level was implemented in monolithic form using a six-way divider/combiner as described above. The second level was in hybrid form where four of the monolithically combined chips were used to make a two stage, two-way power combined amplifier shown in Figure 8. The design used four of the monolithically combined chips described above. The two stage configuration was used to increase the available gain of the combined

amplifiers to compensate for the loss of the two-way divider/combiner.

The two-way divider/combiner consisted of a compensated in-line quarter-wave resistive power splitter (5). The power splitter was constructed on a 100 μm thick semi-insulating GaAs substrate. The measured loss of this power splitter was 0.5 dB for the divider and 0.5 dB for the combiner. A 90 degree offset between the two arms was included to offset any mismatch and obtain a better input and output VSWR. Due to biasing considerations a dc blocking capacitor was used to isolate the first stage from the second. The first and second stages were biased separately to maximize the gain since they operate at different power levels. The performance of this two stage two-way combined amplifier is shown in Figure 9. Under power conditions the chip can deliver 1 W (30 dBm) with 5 dB gain and 5.8% power-added efficiency. Under lower power conditions and with the bias adjusted for maximum gain the chip has 7.5 dB gain with 0.56 W (27.5 dBm) power output.

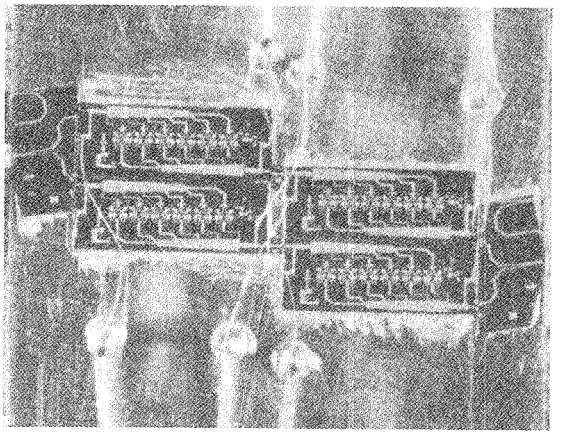

Figure 8. Picture for the two stage two-way combined Ka-band 1 Watt power amplifier module.

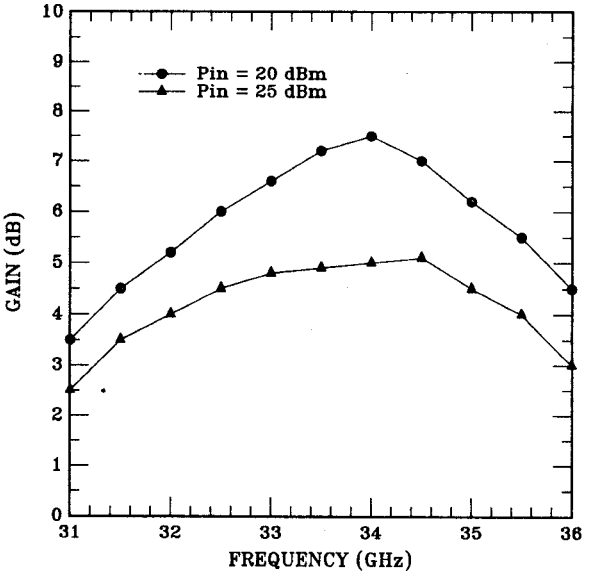

Figure 9. Gain curve for the two stage two-way combined power amplifier module.

CONCLUSION

State of the art power output using an FET amplifier has been achieved at 34 GHz. Power combining of several Ka-band devices has been demonstrated in both monolithic and hybrid form. Six power combined devices in monolithic form can deliver 0.6 W and a hybrid combined amplifier using this chip delivers 1 W of output power. Cascading of these monolithic amplifiers has been successfully demonstrated.

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REFERENCES

1. B. Kim, H.M. Macksey, H.Q. Tserng, H.D. Shih, and N. Camilleri, "Millimeter-wave monolithic GaAs power FET amplifiers," GaAs IC Symposium Tech. Digest, 1986, pp. 61-63.

2. B. Kim, H.M. Macksey, H.Q.Tserng, H.D. Shih, and N. Camilleri, "mm-wave monolithic GaAs power FET amplifiers," Microwave Journal, March 1987, pp. 153-164.

3. A.G.Bert, and D. Kaminsky, "The traveling-wave power divider/ combiner,"IEEE MTT-Symposium Digest, 1980, pp.487-489.

4. H.Q. Tserng, and P. Saunier, "10-30 GHz monolithic GaAs travelling-wave divider/combiner," Electron. Lett., 1985, 21, pp. 950-951.

5. H. Howe, "Stripline circuit design," Artech House, Inc., Massachusetts, 1974, pp. 94-95.